AMENDMENT(S) TO THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims on the application. All claims are set forth below with one of the following annotations.

- (Original): Claim filed with the application.
- (Currently amended): Claim being amended in the current amendment paper.
- (Canceled): Claim cancelled or deleted from the application. No claim text is shown.
- (Withdrawn): Claim still in the application, but in a non-elected status.
- (New): Claim being added in the current amendment paper.
- (Previously presented): Claim added or amended in an earlier amendment paper.
- (Not entered): Claim presented in a previous amendment, but not entered or whose entry status unknown. No claim text is shown.

1. (Currently amended) In a receiving node of a wireless network that is able to receive packets that exactly or substantially conform to a wireless network standard, each packet including a header that includes, in the case that the packet exactly conforms to the standard, reserved bit locations set ~~to bits having respective~~ correct values~~, including~~ and ~~unused bits~~ reserved bit locations set to ~~a known value and combinations of bits being expected~~ one of a plurality of correct combinations, a method comprising:

receiving a start-of-packet (SOP) trigger that indicates that a packet may have been received ;

checking one or more bits in respective ~~unused bits~~ reserved bit locations in the header to determine whether or not they have their respective correct values,

continuing to process the packet in the case that the checking indicates that the checked ~~unused~~ bits have their respective ~~preset~~ correct values.

2. (Currently amended) A method as recited in claim 1, wherein the header of a packet receivable by the node includes a first field modulated at a known rate and including one or more ~~unused bits~~ reserved bit locations, and a second field modulated at a data rate indicated in the first field, the checking including:

processing the first field and checking one or more bits in the first field to determine whether or not they have their respective correct values; and

if the checked bits of the first field have their respective correct values, checking the second field for integrity.

3. (Currently amended) A method as recited in claim 2, wherein the checking one or more bits in the first field to determine whether or not they have their respective correct values includes checking one or more ~~unused bits~~ reserved bit locations of the first field to determine whether or not they ~~have~~ contain their respective correct values.

4. (Original) A method as recited in claim 2, wherein the checking one or more bits in the first field to determine whether or not they have their respective correct values includes checking whether or not one or more combinations of bits in the first field are unexpected.

5. (Currently amended) A method as recited in claim 2, wherein the packet optionally includes an indication of whether or not ~~unused bits~~ reserved bit locations of the second field include an error detecting code formed from at least part of the first field, and wherein the checking the second field for integrity includes:

checking the indication to ascertain whether or not ~~unused bits~~ reserved bit locations of the second field include an error detecting code;

if it is ascertained that such an error detecting code is included, checking the included error correcting code; and

if it is ascertained that an error detecting code is not included, checking one or more ~~unused bits~~ reserved bit locations in the second field to determine whether or not they have their respective ~~preset~~ correct values.

6. (Currently amended) A method as recited in claim 2, wherein the checking the second field for integrity includes:

checking one or more ~~unused bits~~ reserved bit locations in the second field to determine whether or not they have their respective preset values.

7. (Currently amended) A method as recited in claim 2, wherein the receiving node is able to receive packets that conform to one or more of the IEEE 802.11 OFDM standards, wherein the first field is a SIGNAL field ~~modulated at a known data rate~~ and wherein the second field is a SERVICE field ~~modulated at a data rate indicated in the SIGNAL field~~.

8. (Original) A method as recited in claim 2, further comprising:

providing a measure of the received signal quality; and

checking whether the received signal quality measure is above a set level,

such that the SOP trigger is ascertained to be a false trigger in the case that the received signal quality measure is not above the set level.

9. (Original) A method as recited in claim 8, wherein the measure of the received signal quality is a measure of the error vector magnitude (EVM).

10. (Original) A method as recited in claim 8, wherein the measure of the received signal quality is a measure of the signal to adjacent-channel-interference ratio.

11. (Original) A method as recited in claim 2, wherein the receiving node includes a PHY processor and a MAC processor; and wherein the checking of the one or more bits in the first field occurs in the PHY processor.

12. (Currently amended) A method as recited in claim 2, wherein the receiving node includes a PHY processor and a MAC processor; and wherein processing of the first field is by the PHY processor and includes providing the processed data of the first field to the MAC processor, and wherein the checking of the one or more bits in the first field includes the MAC processor accepting the processed data of the first field and checking the one or more bits in the first field.

13. (Original) A method as recited in claim 9, wherein the receiving node includes a PHY processor and a MAC processor; and wherein the PHY processor provides a measure of the EVM to the MAC processor, such that the checking of whether the received EVM is above a set level includes the MAC processor accepting the EVM measure from the PHY processor and checking whether accepted received EVM is above the set level.

14–15. (Cancelled)

16. (Currently amended) A PHY processor ~~as recited in claim 15,~~ of a node of a wireless network to wirelessly receive packets that exactly or substantially conform to a wireless network standard, each packet including a header that includes, in the case that the packet exactly conforms to the standard, reserved bit locations set to correct values and bits set to one of a plurality of correct combinations, the receiving node including a MAC processor having an input coupled to the output of the PHY processor, the header of a packet receivable by the node including a first field modulated at a known rate and including one or more reserved first field bit locations, and a second field modulated at a data rate indicated in the first field, the PHY processor comprising:

an SOP detector to provide a start-of-packet (SOP) trigger that indicates that a packet may have been received;

a receive signal processor to process modulated packet data and provide the processed data to the MAC processor; and

a receive controller coupled to the SOP detector and the receive signal processor, the receive controller configured to:

accept an SOP trigger from the SOP detector that indicates that a packet may have been received;

after such an SOP trigger is accepted, check one or more bits in the header to determine whether or not they have their respective correct values,

wherein the checking ~~one or more bits in the first field to determine whether or not they have their respective correct values~~ by the receive controller includes:

after the receive processor processes the first field, checking one or more bits in the first field to determine whether or not they have their respective correct values, including checking one or more ~~unused bits~~ reserved first field bit locations ~~of the first field~~ to determine whether or not they have their respective preset values; and

if the checked bits of the first field have their respective correct values, checking the second field for integrity,

such that the checking indicates whether or not the SOP trigger is a false SOP trigger.

17. (Cancelled).

18. (Currently amended) (Currently amended) A PHY processor ~~as recited in claim 15, wherein~~ of a node of a wireless network to wirelessly receive packets that exactly or substantially conform to a wireless network standard, each packet including a header that includes, in the case that the packet exactly conforms to the standard, reserved bit locations set to correct values and bits set to one of a plurality of correct combinations, the receiving node including a MAC processor having an input coupled to the

output of the PHY processor, the header of a packet receivable by the node including a first field modulated at a known rate and including one or more reserved first field bit locations, and a second field modulated at a data rate indicated in the first field, the packet optionally ~~includes~~ including an indication of whether or not ~~unused bits~~ reserved bit locations of the second field include an error detecting code formed from at least part of the first field, ~~and~~ the PHY processor comprising:

an SOP detector to provide a start-of-packet (SOP) trigger that indicates that a packet may have been received;

a receive signal processor to process modulated packet data and provide the processed data to the MAC processor; and

a receive controller coupled to the SOP detector and the receive signal processor, the receive controller configured to:

accept an SOP trigger from the SOP detector that indicates that a packet may have been received;

after such an SOP trigger is accepted, check one or more bits in the header to determine whether or not they have their respective correct values,

wherein the checking ~~the second field for integrity~~ by the receive controller includes:

after the receive processor processes the first field, checking one or more bits in the first field to determine whether or not they have their respective correct values; and

if the checked bits of the first field have their respective correct values, checking the second field for integrity including:

checking the indication to ascertain whether or not ~~unused bits~~ reserved bit locations of the second field include an error detecting code;

if it is ascertained that such an error detecting code is included, checking the included error correcting code; and

if it is ascertained that an error detecting code is not included, checking one or more ~~unused bits~~ reserved bit locations in the second field to determine whether or not they have their respective ~~preset~~ correct values,

such that the checking indicates whether or not the SOP trigger is a false SOP trigger.

checking the indication to ascertain whether or not ~~unused bits~~ reserved bit locations of the second field include an error detecting code;

if it is ascertained that such an error detecting code is included, checking the included error correcting code; and

if it is ascertained that an error detecting code is not included, checking one or more ~~unused bits~~ reserved bit locations in the second field to determine whether or not they have their respective ~~preset~~ correct values.

19. (Currently amended) A PHY processor ~~as recited in claim 15,~~ of a node of a wireless network to wirelessly receive packets that exactly or substantially conform to a wireless network standard, each packet including a header that includes, in the case that the packet exactly conforms to the standard, reserved bit locations set to correct values and bits set to one of a plurality of correct combinations, the receiving node including a MAC processor having an input coupled to the output of the PHY processor, the header of a packet receivable by the node including a first field modulated

at a known rate and including one or more reserved first field bit locations, and a second field modulated at a data rate indicated in the first field, the PHY processor comprising:

an SOP detector to provide a start-of-packet (SOP) trigger that indicates that a packet may have been received;

a receive signal processor to process modulated packet data and provide the processed data to the MAC processor; and

a receive controller coupled to the SOP detector and the receive signal processor, the receive controller configured to:

accept an SOP trigger from the SOP detector that indicates that a packet may have been received;

after such an SOP trigger is accepted, check one or more bits in the header to determine whether or not they have their respective correct values,

wherein the checking ~~the second field for integrity~~ by the receive controller includes:

after the receive processor processes the first field, checking one or more bits in the first field to determine whether or not they have their respective correct values; and

if the checked bits of the first field have their respective correct values, checking the second field for integrity, including checking one or more ~~unused bits~~ reserved bit locations in the second field to determine whether or not they have their respective preset values,

such that the checking indicates whether or not the SOP trigger is a false SOP trigger.

20. (Cancelled).

21. (Currently amended) A PHY processor ~~as recited in claim 15, further comprising:~~ of a node of a wireless network to wirelessly receive packets that exactly or substantially conform to a wireless network standard, each packet including a header that includes, in the case that the packet exactly conforms to the standard, reserved bit locations set to correct values and bits set to one of a plurality of correct combinations, the receiving node including a MAC processor having an input coupled to the output of the PHY processor, the header of a packet receivable by the node including a first field modulated at a known rate and including one or more reserved first field bit locations, and a second field modulated at a data rate indicated in the first field, the PHY processor comprising:

an SOP detector to provide a start-of-packet (SOP) trigger that indicates that a packet may have been received;

a receive signal processor to process modulated packet data and provide the processed data to the MAC processor;

a signal quality calculator to provide a measure of the received signal quality; and

a receive controller coupled to the SOP detector and the receive signal processor, the receive controller configured to:

accept an SOP trigger from the SOP detector that indicates that a packet may have been received;

after such an SOP trigger is accepted, check one or more bits in the header to determine whether or not they have their respective correct values;

~~the receive controller further configured to~~

accept the received signal quality measure from the signal quality calculator; and

check whether the received signal quality measure is above a set level,

wherein the checking by the receive controller includes:

after the receive processor processes the first field, checking one or more bits in the first field to determine whether or not they have their respective correct values; and

if the checked bits of the first field have their respective correct values, checking the second field for integrity,

such that the checking indicates whether or not the SOP trigger is a false SOP trigger, and such that the SOP trigger is ascertained to be a false trigger in the case that the received signal quality measure is not above the set level.

22. (Original) A PHY processor as recited in claim 21, wherein the signal quality calculator is an error vector magnitude (EVM) calculator to provide a measure of the error vector magnitude (EVM).

23.–24. (Cancelled).

25. (Currently amended) A control means ~~as recited in claim 24,~~ for inclusion in a receiving node of a wireless network that is able to receive packets that exactly or substantially conform to a wireless network standard, each packet including a header that includes, in the case that the packet exactly conforms to the standard, reserved bit locations set to correct values, and bits set to one of a plurality of correct combinations, the header of a packet receivable by the node including a first field modulated at a known rate and including one or more reserved bit locations, and a second field modulated at a data rate indicated in the first field, a control means comprising:

means for receiving a start-of-packet (SOP) trigger that indicates that a packet may have been received ;

means for checking one or more bits in the header to determine whether or not they have their respective correct values, the means for checking including:

means for checking one or more bits in the first field to determine whether or not they have their respective correct values; and

means for checking the second field for integrity if the checked bits of the first field have their respective correct values; and

means for continuing to process the packet in the case that the checking indicates that the checked bits have their respective correct values,

wherein the packet optionally includes an indication of whether or not ~~unused bits~~ reserved bit locations of the second field include an error detecting code formed from at least part of the first field, and wherein the means for checking the second field for integrity includes:

means for checking the indication to ascertain whether or not ~~unused bits~~ reserved bit locations of the second field include an error detecting code;

means for checking the included error correcting code if it is ascertained that such an error detecting code is included; and

means for checking one or more ~~unused bits~~ reserved bit locations in the second field to determine whether or not they have their respective ~~preset~~ correct values if it is ascertained that an error detecting code is not included.

26. (Currently amended) A control means ~~as recited in claim 24,~~ for inclusion in a receiving node of a wireless network that is able to receive packets that exactly or substantially conform to a wireless network

standard, each packet including a header that includes, in the case that the packet exactly conforms to the standard, reserved bit locations set to correct values, and bits set to one of a plurality of correct combinations, the header of a packet receivable by the node including a first field modulated at a known rate and including one or more reserved bit locations, and a second field modulated at a data rate indicated in the first field, a control means comprising:

means for receiving a start-of-packet (SOP) trigger that indicates that a packet may have been received ;

means for checking one or more bits in the header to determine whether or not they have their respective correct values, the means for checking including:

means for checking one or more bits in the first field to determine whether or not they have their respective correct values; and

means for checking the second field for integrity if the checked bits of the first field have their respective correct values; and

means for continuing to process the packet in the case that the checking indicates that the checked bits have their respective correct values,

wherein the means for checking the second field for integrity includes:

means for checking one or more ~~unused bits~~ reserved bit locations in the second field to determine whether or not they have their respective preset values.

27. (Currently amended) A control means ~~as recited in claim 24,~~ for inclusion in a receiving node of a wireless network that is able to receive packets that exactly or substantially conform to a wireless network

standard, each packet including a header that includes, in the case that the packet exactly conforms to the standard, reserved bit locations set to correct values, and bits set to one of a plurality of correct combinations, the header of a packet receivable by the node including a first field modulated at a known rate and including one or more reserved bit locations, and a second field modulated at a data rate indicated in the first field, a control means comprising:

means for receiving a start-of-packet (SOP) trigger that indicates that a packet may have been received ;

means for checking one or more bits in the header to determine whether or not they have their respective correct values, the means for checking including:

means for checking one or more bits in the first field to determine whether or not they have their respective correct values; and

means for checking the second field for integrity if the checked bits of the first field have their respective correct values;

means for continuing to process the packet in the case that the checking indicates that the checked bits have their respective correct values;

~~further comprising:~~

means for providing a measure of the received signal quality; and

means for checking whether the received signal quality measure is above a set level,

such that the SOP trigger is ascertained to be a false trigger in the case that the received signal quality measure is not above the set level.

28. (Original) A control means as recited in claim 27, wherein the measure of the received signal quality is a measure of the error vector magnitude (EVM).

29. (Currently amended) A carrier medium including one or more computer readable code segments to instruct one or more processors of a processing system to implement a method in a receiving node of a wireless network that is able to receive packets that exactly or substantially conform to a wireless network standard, each packet including a header that includes, in the case that the packet exactly conforms to the standard, reserved bits ~~having respective~~ set to correct values~~, including unused~~ and bits set to ~~a known value and~~ one of a plurality of correct combinations ~~of bits being expected combinations~~, the method comprising:

receiving a start-of-packet (SOP) trigger that indicates that a packet may have been received ;

checking one or more ~~unused bits~~ reserved bit locations in the header to determine whether or not they have their respective correct values,

continuing to process the packet in the case that the checking indicates that the checked bits have their respective correct values.

30. (Currently amended) A carrier medium as recited in claim 29, wherein the header of a packet receivable by the node includes a first field modulated at a known rate and including one or more ~~unused bits~~ reserved bit locations, and a second field modulated at a data rate indicated in the first field, the checking including:

processing the first field and checking one or more bits in the first field to determine whether or not they have their respective correct values; and

if the checked bits of the first field have their respective correct values, checking the second field for integrity.

31. (Currently amended) A carrier medium as recited in claim 30, wherein the packet optionally includes an indication of whether or not ~~unused bits~~ reserved bit locations of the second field include an error detecting code formed from at least part of the first field, and wherein the checking the second field for integrity includes:

checking the indication to ascertain whether or not ~~unused bits~~ reserved bit locations of the second field include an error detecting code;

if it is ascertained that such an error detecting code is included, checking the included error correcting code; and

if it is ascertained that an error detecting code is not included, checking one or more ~~unused bits~~ reserved bit locations in the second field to determine whether or not they have their respective ~~preset~~ correct values.

32. (Currently amended) A carrier medium as recited in claim 30, wherein the checking the second field for integrity includes:

checking one or more ~~unused bits~~ reserved bit locations in the second field to determine whether or not they have their respective preset values.

33. (Currently amended) A carrier medium as recited in claim 30, wherein the receiving node is able to receive packets that conform to one or more of the IEEE 802.11 OFDM standards, wherein the first field is a SIGNAL field ~~modulated at a known data rate~~ and wherein the second field is a ~~SERICE~~ SERVICE field ~~modulated at a data rate indicated in the SIGNAL field~~.